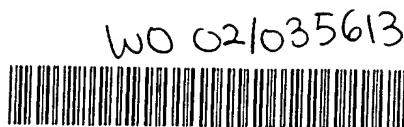


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(74) Representative: **Senior, Alan Murray**
J.A. KEMP & CO.,
14 South Square,
Gray's Inn
London WC1R 5JJ (GB)

(71) Applicant: **Nakata, Josuke**
Jyoyo-shi, Kyoto 610-0102 (JP)

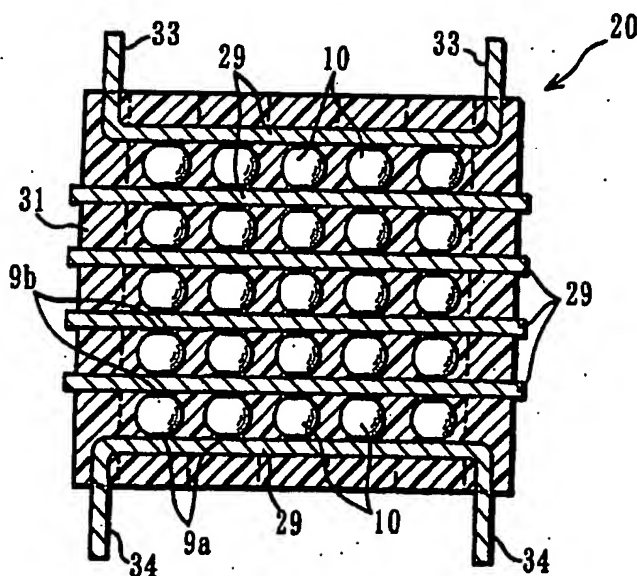
(72) Inventor: **Nakata, Josuke**
Jyoyo-shi, Kyoto 610-0102 (JP)

(54) **LIGHT-EMITTING OR LIGHT-DETECTING SEMICONDUCTOR MODULE AND METHOD OF MANUFACTURE THEREOF**

(57) In a semiconductor module (20), twenty-five semiconductor devices (10) having light-receiving properties, for example, are arranged in five-by-five matrices using a conductor mechanism formed from six lead frames (29). Each column of semiconductor devices (10) is connected in series and each row of semicon-

ductor devices (10) is connected in parallel. These are embedded in a light-transmitting member (31) formed from a transparent synthetic resin, and a positive electrode terminal 33 and a negative electrode terminal 34 are disposed. The semiconductor devices (10) are formed with first and second flat surfaces, and negative electrodes 9a and positive electrodes 9b are disposed.

FIG. 14



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Description

BACKGROUND OF THE INVENTION

[0001] The present invention relates to a light-emitting or light-receiving module equipped with a plurality of particle-shaped semiconductor devices and a method for making the same. This light-emitting or light-receiving semiconductor module can be used in various applications such as solar cell panels, illumination panels, displays, semiconductor photocatalysts, and the like.

[0002] Research has been done in technologies wherein a pn junction separated by a diffusion layer is formed on the surface of a small, spherical semiconductor element formed from p-type or n-type semiconductors. Multiple spherical semiconductor elements of this type are connected in parallel to a shared electrode to be used in solar cells and semiconductor photocatalyst.

[0003] United States Patent No. 3,998,659 discloses an example of a solar cell. A p-type diffusion layer is formed on the surface of a n-type spherical semiconductor, and multiple spherical semiconductors of this type are connected to a shared electrode film (positive electrode) while the n-type cores of these spherical semiconductors are connected to a shared electrode film (negative electrode).

[0004] In United States patent No. 4,021,323, p-type spherical semiconductor elements and n-type spherical semiconductor elements are arranged in a matrix and connected to a shared electrode film. These semiconductor elements are also placed in contact with an electrolytic fluid. This results in a solar energy converter (semiconductor module) where electrolysis of the electrolyte takes place when illuminated with sunlight. United States patent No. 4,100,051 and 4,136,436 present similar solar energy converters.

[0005] In these types of conventional semiconductor modules, the semiconductor elements are connected in parallel. Thus, a low voltage and a high current is applied to the terminals of the module. If one of the semiconductor elements malfunctions and results in a short-circuit, a high current will pass through this short-circuit and output from the module will be lost.

[0006] As presented in PCT gazettes WO98/15983 and WO99/10935, the inventor of the present invention proposed a light-emitting or light-receiving semiconductor element wherein a diffusion layer, a pn junction, and a pair of electrodes are formed on a spherical semiconductor made from a p-type semiconductor and a n-type semiconductor. These multiple semiconductor elements of this type can be connected in series, and these series can be connected in parallel to form solar cells, photocatalyst devices involving the electrolysis of water and the like, as well as various types of light-emitting devices, color displays, and the like.

[0007] In these semiconductor modules, if any one of the elements connected in series malfunctions, an open circuit will result and current will not flow through the se-

ries circuit that includes the semiconductor element. As a result, the remaining operating semiconductor devices in the series circuit will also be stopped, lowering the output of the semiconductor module.

[0008] Furthermore, in the spherical semiconductor device with positive and negative electrodes proposed by the present inventor in the publications described above, the semiconductor device can roll around easily, making handling difficult. Determining the positions at which the positive and negative electrodes are formed is not easy and identifying polarity during assembly is difficult.

OBJECTS AND SUMMARY OF THE INVENTION

[0009] An object of the present invention is to provide a light-emitting or light-receiving semiconductor module that can minimize reductions in output voltage and current in the event of a malfunction in a device and a method for making the same. Another object of the present invention is to provide a light-emitting or light-receiving semiconductor module that allows easy identification of a pair of electrodes on a particle-shaped semiconductor device and a method for making the same. Yet another object of the present invention is to provide a light-emitting or light-receiving semiconductor module that uses reflections from a light-transmitting member to guide light to positions away from the entry point or light source point and a method for making the same.

[0010] A light-emitting or light-receiving module according to the present invention includes: a plurality of particle-shaped semiconductor devices having light-emitting or light-receiving properties, the plurality of semiconductor devices being disposed in plural rows and columns with uniform conductive orientation; and a conductive connection mechanism connecting each of the columns of the plurality of semiconductor devices to be electrically in series and connecting each of the rows of the plurality of semiconductor devices to be electrically in parallel (claim 1).

[0011] It would be desirable for the conductive connection mechanism to be formed from a plurality of lead frames formed from thin metal sheets (claim 2). Also, a light-transmitting member covers all of the semiconductor devices and all of the semiconductor devices are embedded therein (claim 3).

[0012] In the light-emitting or light-receiving module described in claim 1, preferably, the semiconductor device is a solar cell (claim 4). Alternatively, the semiconductor device can be a spherical semiconductor device (claim 5), or the semiconductor device can be a cylindrical semiconductor device (claim 6).

[0013] In the light-emitting or light-receiving module described in claim 2, it would be desirable for the semiconductor device to be a roughly spherical semiconductor element formed from a p-type or n-type semiconductor, the semiconductor element being formed with parallel first and second flat surfaces on either side of a

center thereof; a roughly spherical pn junction is formed on a surface section of the semiconductor element including the first flat surface; and first and second electrodes are disposed on the first and second flat surfaces respectively and connected to ends of the pn junction (claim 7).

[0014] In the light-emitting or light-receiving module described in claim 2, it would be desirable for the semiconductor device to be a cylindrical semiconductor element formed from a p-type or n-type semiconductor, the semiconductor element being formed with parallel first and second flat surfaces perpendicular to an axis thereof; a pn junction is formed on a surface section of the semiconductor element including the first flat surface; and first and second electrodes are disposed on the first and second flat surfaces respectively and connected to ends of the pn junction (claim 8).

[0015] In the light-emitting or light-receiving module described in claim 7, it would be desirable for an average diameter of the first and second flat surfaces to be smaller than a distance between the flat surfaces (claim 9). Alternatively, the first and second flat surfaces can be formed with different diameters (claim 10).

[0016] In the light-emitting or light-receiving module described in claim 7 or claim 8, it would be desirable for the semiconductor element to be formed from a silicon semiconductor (claim 11). Alternatively, the semiconductor element is formed from any one of compound semiconductor selected from GaAs, InP, GaP, GaN, or InCuSe (claim 12). Alternatively, the semiconductor element is formed from a p-type semiconductor; the diffusion layer is formed from a n-type diffusion layer; and the second flat surface is formed from a p-type recrystallized layer, a second electrode being disposed on a surface of the p-type recrystallized layer (claim 13). Alternatively, the semiconductor element is formed from a n-type semiconductor; the diffusion layer is formed from a p-type diffusion layer; and the second flat surface is formed from a n-type recrystallized layer, a second electrode being disposed on a surface of the n-type recrystallized layer (claim 14).

[0017] Another light-emitting or light-receiving module according to the present invention includes: a plurality of particle-shaped semiconductor devices having light-emitting or light-receiving properties, the plurality of semiconductor devices being disposed in a plurality of columns with uniform conductive orientation and being disposed in ring formations at equal intervals along a perimeter; and a conductive connection mechanism connecting each of the columns of the plurality of semiconductor devices to be electrically in series and connecting each of the rings of the plurality of semiconductor devices to be electrically in parallel (claim 15).

[0018] It would be desirable for a cylindrical light-transmitting member formed from a transparent synthetic resin to be provided; and the plurality of columns of semiconductor devices arranged in ring formations to be embedded in perimeter walls of the light-transmitting

member (claim 16). It would be desirable for an irregular reflection surface that irregularly reflects light to be formed on an inner perimeter surface of the light-transmitting member (claim 17, dependent on claim 16).

[0019] A method for making a light-emitting or light-receiving module according to the present invention includes: a first step for preparing a plurality of lead frames formed from thin metal sheets and a plurality of particle-shaped semiconductor devices having light-emitting or light-receiving properties; a second step for assembling the plurality of semiconductor devices between the plurality of lead frames so that conductive orientation is uniform, arranging the semiconductor devices as a matrix with plural rows and plural columns, and connecting each column of the semiconductor devices via the lead frame to be electrically in series and connecting each row of the semiconductor devices via the lead frame to be electrically in parallel; and a third step for embedding the matrix of the plurality of semiconductor devices in a light-transmitting member formed from a transparent synthetic resin (claim 18).

[0020] It would be desirable in the third step for partially cylindrical lenses to be formed on either side of each of the columns of the semiconductor devices (claim 19).

[0021] According to another method for making a light-emitting or light-receiving module according to the present invention, there is: a first step for preparing a plurality of ring-shaped lead frames formed from thin metal sheets and a plurality of particle-shaped semiconductor devices having light-emitting or light-receiving properties; a second step for assembling the plurality of semiconductor devices between the plurality of lead frames so that conductive orientation is uniform, arranging the semiconductor devices in a plurality of columns and in ring formations at equal intervals along a perimeter, and connecting each column of the semiconductor devices via the lead frame to be electrically in series and connecting each ring of the semiconductor devices via the lead frame to be electrically in parallel; and a third step for embedding the plurality of columns of the plurality of semiconductor devices in a cylindrical light-transmitting member formed from a transparent synthetic resin (claim 20).

BRIEF DESCRIPTION OF THE DRAWINGS

[0022]

Fig. 1 through Fig. 16 are drawings showing the first embodiment.

Fig. 1 is a cross-section drawing of a spherical semiconductor element.

Fig. 2 is a cross-section drawing of the semiconductor element formed with a first flat surface.

Fig. 3 is a cross-section drawing of a semiconductor element formed with a diffusion layer and a pn junction.

Fig. 4 is a cross-section drawing of a semiconductor element formed with a second flat surface.

Fig. 5 is a cross-section drawing of a semiconductor element formed with a diffusion layer.

Fig. 6 is a cross-section drawing of a semiconductor device.

Fig. 7 is a plan drawing of a lead frame plate.

Fig. 8 is a cross-section drawing of an assembly in which semiconductor devices have been assembled with a lead frame plate.

Fig. 9 is a cross-section detail drawing of a semiconductor device and a lead frame.

Fig. 10 is a plan drawing of three sets of semiconductor modules and lead frame plates.

Fig. 11 is a cross-section drawing of a semiconductor module and lead frame plate.

Fig. 12 is a cross-section drawing of a semiconductor module and lead frame plate.

Fig. 13 is a plan drawing of a semiconductor module.

Fig. 14 is a cross-section drawing of a semiconductor module.

Fig. 15 is a side-view drawing of a semiconductor module.

Fig. 16 is an equivalent circuit diagram of a semiconductor module.

Fig. 17 is a cross-section drawing of a semiconductor device according to an alternative embodiment 1.

Fig. 18 through Fig. 21 are drawings showing an alternative embodiment 2.

Fig. 18 is a cross-section drawing of a semiconductor element formed with first and second flat surfaces.

Fig. 19 is a cross-section drawing of a semiconductor element formed with a diffusion layer.

Fig. 20 is a cross-section drawing of a semiconductor element formed with a negative electrode.

Fig. 21 is a cross-section drawing of a semiconductor device.

Fig. 22 through Fig. 30 show an alternative embodiment 3.

Fig. 22 is a drawing showing a cylindrical semiconductor material and a semiconductor element.

Fig. 23 is a cross-section drawing along the XXI-II-XXIII line from Fig. 22.

Fig. 24 is a cross-section drawing of a semiconductor element formed with a diffusion layer.

Fig. 25 is a cross-section drawing of a semiconductor element with a flat surface removed.

Fig. 26 is a cross-section drawing of a semiconductor element formed with a diffusion layer.

Fig. 27 is a cross-section drawing of a semiconductor device.

Fig. 28 is a plan drawing of a semiconductor module.

Fig. 29 is a cross-section drawing along the XXVIII-XXVIII line from Fig. 28.

Fig. 30 is a simplified cross-section detail drawing of a semiconductor device and lead frame.

Fig. 31 through Fig. 34 show an alternative embodiment 4.

Fig. 31 is a plan drawing of an assembly during the process of making a semiconductor module.

Fig. 32 is a front-view drawing of an assembly.

Fig. 33 is a plan drawing of a semiconductor module.

Fig. 34 is a cross-section drawing of a semiconductor module.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0023] Referring to the figures, the embodiments of the present invention will be described.

[0024] First, the structure of a semiconductor device according to the present invention will be described.

[0025] Referring to Fig. 1 through Fig. 6, there is shown a method for making a light-receiving semiconductor device 10 suited for solar cells. Referring to Fig. 6, there is shown a cross-section drawing of the light-receiving semiconductor device 10.

[0026] Referring to Fig. 6, the light-receiving semiconductor device 10 is formed from: a semiconductor element 1 formed, for example, from a p-type semiconductor; a n-type diffusion layer 3; a pn junction 4; a pair of electrodes 9a, 9b (a negative electrode 9a, a positive electrode 9b); a diffusion layer 8 formed from a type-p+ semiconductor; and a reflection prevention film 6a. The semiconductor element 1 is formed from a perfectly spherical semiconductor element 1a (see Fig. 1) formed from a p-type silicon single crystal with a diameter of, for example, 1.5 mm. At a pair of apexes on either side of the center of the semiconductor element 1 are formed first and second flat surfaces 2, 7, which are parallel to each other. The first flat surface 2 has a diameter of, for example, 0.6 mm. The second flat surface 7 has a diameter of, for example, 0.8 mm. The average diameter of the first flat surface 2 and the second flat surface 7 is smaller than the distance between the first flat surface 2 and the second flat surface 7.

[0027] The diffusion layer 3 is formed on a section of the surface of the semiconductor element 1 that includes the first flat surface 2. A n-type diffusion layer 3 is not formed on the second flat surface 7, and instead another diffusion layer 8 is formed. The diffusion layer 3 is a type-n+ diffusion layer formed through phosphorous diffusion and having a thickness of 0.4 - 0.5 microns. The pn junction 4 (more precisely, a pn+ junction) is formed roughly spherically, with the diffusion layer 3.

[0028] On the first flat surface 2, the negative electrode 9a is formed as a thin film on the surface of the diffusion layer 3 by baking a silver paste. On the second flat surface 7, the positive electrode 9b is formed as a thin film on the surface of the type-p+ diffusion layer 8 by baking a silver paste. The reflection-prevention film

conductor modules 20 are separated. First, for the middle lead frame plates 22 - 25, cutting areas 32 at the ends of the lead frames 29 extending from the light-transmitting members 31 are cut by the molding die. For the top and bottom lead frame plates 21, 26, the cutting areas of the lead frames 29 are cut from the outer frame 28 leaving them to extend out from the light-transmitting member 31.

[0048] Next, different alternatives involving partial modifications to the above embodiment will be presented.

1) Alternative embodiment 1 (Fig. 17)

[0049] Referring to Fig. 17, a semiconductor device 10A is formed with a positive electrode 9c, in which an aluminum ball is bonded to the second flat surface 7. The type-p+ diffusion layer 8 described above is omitted. To produce this semiconductor device 10, the steps illustrated in Fig. 1 through Fig. 4 are performed. Then, with the negative electrode 9a bonded to the lead frame 29 with solder 11, an aluminum ball having a diameter of 0.3 - 0.4 mm is bonded to the center of the second flat surface 7 via ultrasound and heat, thus forming the positive electrode 9c, in the form of a bump.

[0050] It would also be possible to use a gold ball in place of the aluminum ball described above. Electrodes formed via ball bonding in this manner are suited for accurate electrode formation in a small space and low-resistance contacts can be formed at lower temperatures compared with using diffusion or alloys. Since the height of the positive electrode 9c can be increased, it is possible to increase the space between the lead frames 29 or the space between the semiconductor device electrodes when semiconductor devices are connected in series. Thus, a conductive adhesive can be applied to just the positive electrode 9c. Also, this positive electrode 9c can be implemented for the semiconductor device 10 described above. Also, the semiconductor device 10A described here can be used in the semiconductor module 20 in place of the semiconductor device 10.

2) Alternative embodiment 2 (Fig. 18 - Fig. 21)

[0051] Referring to Fig. 18 through Fig. 21, a method for making a semiconductor device 10B will be described. Referring to Fig. 18, a semiconductor element 1B is formed as in the embodiment described above. First and second flat surfaces 2, 7b are formed parallel to each other at the two ends on either side of the center of a spherical semiconductor element 1a (1.5 mm diameter) formed from a p-type silicon single crystal (1 ohm-m resistivity). The diameters of the first and second flat surfaces 2, 7b are approximately 0.6 mm and 0.8 mm respectively, and the average diameters of the first and second flat surfaces 2, 7b are smaller than the distance between the first and second flat surfaces 2, 7b. Refer-

ring to Fig. 19, phosphorous is dispersed as a n-type dopant over the entire surface of the semiconductor element 1B to form a type-n+ diffusion layer 3 having a thickness of approximately 0.4 - 0.5 microns.

[0052] Referring to Fig. 20, the silicon oxide film generated during the diffusion of phosphorous is removed by etching. Referring to Fig. 21, a silver paste is printed on the center of the first flat surface 2 as a dot having a diameter of 0.4 mm and a thickness of 0.2 mm. This silver paste is heated under an oxidizing gas or an inert gas atmosphere at a temperature of 600 - 800 deg C, resulting in a negative electrode 9a that forms a low-resistance connection with the diffusion layer 3. Next, an aluminum dot having a diameter of approximately 0.4 mm and a thickness of approximately 0.3 mm is placed on the surface of the second flat surface 7b and is heated rapidly to a temperature of 750 - 850 deg C under an inert gas atmosphere or in a vacuum. As a result, the silicon melted by the eutectic reaction of the aluminum and the silicon grows into a type-p+ recrystallized layer 8b doped with aluminum, with the silicon single crystal serving as a seed. This technology is known as alloy pn-junction forming.

[0053] Since the recrystallized layer 8b passes through the diffusion layer 3, the aluminum remaining on the surface forms a negative electrode 9d via the p-type silicon single crystal section and the type-p+ recrystallized layer 8b. The pn junction 4b is connected to the p+n+ junction 4d. An anti-reflection film for the semiconductor element 1B is then formed.

[0054] With this semiconductor element 1B, the type-p+ recrystallized layer 8b and the positive electrode 9d can be formed at the same time without requiring boron diffusion as in the semiconductor device 10 described above. Since the height of the positive electrode 9d is increased, conductive adhesive can be applied without affecting the surface of the recrystallized layer 8b.

[0055] In place of the aluminum described above, it would also be possible to form the recrystallized layer 8b and the positive electrode 9d at the same time using gold (AuB) formed with a molecular ratio of approximately 99% gold and 1% boron. Alternatively gold (Au-Ga) with a ratio of 99% gold and 1% gallium could be used. Also, this semiconductor device 10B can be used in the semiconductor module 20 in place of the semiconductor device 10 described above.

3) Alternative embodiment 3 (Fig. 22 - Fig. 30)

[0056] Referring to Fig. 27, a light-receiving semiconductor device 10C suited for use in solar cells includes: a cylindrical semiconductor element 41; first and second flat surfaces 42, 43 thereof; a n-type diffusion layer 44; a pn junction 45; a type-p+ diffusion layer 47; a silicon oxide film 46 serving as a reflection prevention film; a negative electrode 49a; and a positive electrode 49b. This semiconductor device 10C is formed as a short cylinder. While having a different shape from the semicon-

multiple columns with their conductivity directions aligned (in this embodiment, five rows and five columns). By the conductive connector mechanism, the semiconductor devices 10 in each column are connected electrically in series, and the semiconductor devices 10 in each row are connected electrically in parallel. The conductive connector mechanism is formed from six metallic lead frames 29. A lead frame 29 is mounted between adjacent rows of semiconductor devices 10 and forms electrical connections with the electrodes 9a, 9b. The lead frame 29 that is integral with the negative electrode terminals 34 at the bottom end is electrically connected in parallel with the electrodes 9a of the semiconductor devices 10 of the first row. The lead frame 29 that is integral with the positive electrode terminals 33 at the top end is electrically connected in parallel with the electrodes 9b of the semiconductor devices 10 of the fifth row. These twenty-five semiconductor devices 10 and the conductive connector mechanism can be, for example, embedded in a light-transmitting member 31 and covered. The light-transmitting member 31 is formed from a transparent synthetic resin such as an acrylic resin or polycarbonate. The light-transmitting member 31 is formed with semi-cylindrical lenses 31a for introducing sunlight from either side of semiconductor devices 10. These semi-cylindrical lenses 31a serve to efficiently introduce sunlight to the columns of the semiconductor devices 10. Compared to a flat structure, a wider orientation brings superior light collection, light focusing, and light guiding properties.

[0039] Referring to Fig. 16, there is shown an electrical circuit that is equivalent to the light-receiving semiconductor module 20 used in a solar cell panel as described above. The twenty-five semiconductor devices 10 form a five-by-five matrix, and the rows of semiconductor devices 10 is connected electrically in series by the six lead frames 29. The rows of semiconductor devices 10 are connected electrically in parallel by the lead frames 29.

[0040] If one of the semiconductor devices 10 in this semiconductor module 20 malfunctions and stops working, light-generated power will simply stop from the malfunctioning semiconductor device 10 while the other functioning semiconductor devices 10 will continue to operate normally and generate electricity. The generated electricity is reliably output through the positive electrode terminal 33 and the negative electrode terminal 34 so that the light-receiving semiconductor module 20 will provide superior reliability and longevity.

[0041] Referring to Fig. 7 through Fig. 12, a method for making the light-receiving semiconductor module 20 (solar cell module) presented above will be described.

[0042] First, the semiconductor devices 10 described above are made. Referring to Fig. 7, lead frame plates 21 - 26 formed with four openings 27a, 27b are made by using a die to punch thin iron-nickel alloy (56% Fe, 42% Ni) plates (thickness of approximately 0.3 mm) with silver surface plating approximately 3 microns thick.

Wide (approximately 4 mm) outer frames 28 and three parallel narrow (1.5 mm) lead frames 29 are formed on the lead frame plates 21 - 26. The ends of the top and bottom lead frame plates 21, 26 are bent beforehand at right angles, and the inner four lead frame plates 22 - 25 are formed as flat sheets.

[0043] Referring to Fig. 7 through Fig. 9, a conductive adhesive 30a (e.g., a silver epoxy resin) is used on the lead frames 29 of the lead frame plates 21 - 25 so that sets of five semiconductor devices 10 can be adhered at an even pitch with their negative electrode 9a facing down.

[0044] Next, a conductive adhesive 30b is applied on the positive electrodes 9b of the semiconductor devices 10 on the lead frames 29. Referring to Fig. 8, the lead frame 29 of the lead frame plate 22 is placed on top of the positive electrodes 9b of the fifteen (three sets of five) semiconductor devices 10 on the bottom layer. The lead frame plates 23 - 26 are subsequently stacked in sequence in a similar manner, thus forming a regularly arranged five-by-five matrix with each set of twenty-five semiconductor devices 10 being aligned with the other sets. Next, in order to provide electrical connections for the positive electrode 9b and the negative electrode 9a of each of the semiconductor devices 10 to the lead frames 29 above and below it, a weight (not shown in the figure) having a predetermined weight is placed on the uppermost lead frame plate 26 and heat of approximately 160 - 180 deg C is applied to set the adhesive.

[0045] In this manner, the sets (modules) of twenty-five semiconductor devices 10 are electrically connected by the six lead frame plates 21 - 26, and three sets with a total of 75 semiconductor devices 10 are arranged in a regular manner between the lead frames 29 of the six lead frame plates 21 - 26. Within the sets of 25 semiconductor devices 10, the semiconductor devices 10 in each column are connected electrically in series by the lead frames 29, and the semiconductor devices 10 in each row are electrically connected in parallel. Referring to Fig. 9, there is shown a detail drawing of a semiconductor device 10 and the lead frames 29 above and below it.

[0046] Referring to Fig. 10 through Fig. 12, an assembly 30 formed from the 75 semiconductor devices 10 and the six lead frame plates 21 - 26 is housed in a molding die (not shown in the figure) and a transparent synthetic resin (e.g., an acrylic resin or a polycarbonate) is used to form a mold. This results in the five-by-five matrices of semiconductor devices 10 and their corresponding lead frames 29 being embedded in and covered by the light-transmitting members 31 formed from the transparent synthetic resin as described above. In this manner, three sets of solar panels, i.e., light-receiving semiconductor modules 20, are formed at once. The light-transmitting members 31 are formed with partially cylindrical lenses 31a that focus sunlight from either side of the rows of the semiconductor devices 10.

[0047] Finally, the three sets of light-receiving semi-

6a is formed from a silicon oxide film 6 and is formed over the surface of the diffusion layer 3 with the exception of the first flat surface 2 and the second flat surface 7. The structure of the light-receiving semiconductor device 10 will become further evident in the description of the method for making the light-receiving semiconductor device 10 provided below.

[0029] In this light-receiving semiconductor device 10, the roughly spherical pn junction 4 has a photoelectrical conversion function and photoelectrically converts received sunlight to an electric power of approximately 0.6 volts. Since the negative electrode 9a and the positive electrode 9b are formed as thin films on the first and the second flat surfaces 2, 7, the light-receiving semiconductor device 10 is prevented from easily rolling around while allowing it to be easily grasped from both sides, thus making handling easier. Furthermore, since the first flat surface 2 and the second flat surface 7 have different sizes, the negative electrode 9a and the positive electrode 9b can be easily distinguished either visually or through a sensor. This makes assembly of the light-receiving semiconductor device 10 into semiconductor modules more efficient.

[0030] Referring to Fig. 1 through Fig. 6, a method for making the light-receiving semiconductor device 10 presented above will be described. Referring to Fig. 1, a spherical semiconductor element 1a is produced as a true sphere formed from a p-type silicon of single crystal with a resistivity of approximately 1 ohm-meter. This type of spherical semiconductor element 1a can be made using methods proposed in Japanese laid-open patent publication No. 10-33969 and International gazette WO98/15983. In this method, a silicon particle is melted inside the upper end of a drop tube. The silicon particle is dropped down and solidifies while free falling to form a spherical shape due to surface tension, thus forming a spherical silicon single crystal. It would also be possible to form spherical semiconductors by performing mechanical polishing or the like.

[0031] Referring to Fig. 2, mechanical and chemical grinding is performed on a section of the surface of the spherical semiconductor element 1a to form the first flat surface 2 having a diameter of approximately 0.6 mm. Referring to Fig. 3, a method known in the art is used to diffuse phosphorous over the entire surface to form an n+ diffusion layer 3, resulting in a roughly spherical pn junction 4 positioned at a depth of about 0.4 - 0.5 microns from the surface of the spherical semiconductor element 1. A silicon oxide film 5 formed on the surface during the phosphorous diffusion process is removed through etching, and heat is applied again under an oxygen atmosphere to form a silicon oxide film 6 (reflection prevention film 6a).

[0032] Referring to Fig. 4, the side opposite from the first flat surface 2 is processed through mechanical and chemical grinding to form the second flat surface 7, where the p-type silicon single crystal is exposed with a diameter of approximately 0.8 mm. The first and the sec-

ond flat surfaces 2, 7 are formed parallel at end points on either side of the center of the sphere. The diameter of the second flat surface 7 is formed different from the diameter of the first flat surface 2, allowing easy identification of the negative electrode 9a and the positive electrode 9b when connecting lead frames, described later.

[0033] Referring to Fig. 5, using a method known in the field, after forming the first and the second flat surfaces 2, 7 and masking the silicon oxide film 6, the boron is diffused over the surface of the p-type silicon single crystal exposed at the second flat surface 7 to form a type-p+ diffusion layer 8 having a thickness of 0.2 - 0.3 microns. The boron is diffused over the p-type layer on the second flat surface 7, and a p+n+ junction 8a that is in contact with the type-n+ diffusion layer 3 at the edges of the second flat surface 7 is formed inside the silicon oxide film 6. The surface of the p+n+ junction 8a is protected by the silicon oxide film 6.

[0034] Referring to Fig. 6, a silver paste is applied to the surface of the diffusion layer 3 on the first flat surface 2 and the surface of the diffusion layer 8 on the second flat surface 7. The silver paste layers are heated and baked at a range of 600 - 800 deg C under an oxidizing atmosphere. This results in the negative electrode 9a and the positive electrode 9b, which form low-resistance connections with the diffusion layer 3 and the type-p+ diffusion layer 8 respectively. This completes a particle-shaped light-receiving semiconductor device 10 suited for solar cells.

[0035] The production method described above is just one example. The processes for forming the type-n+ diffusion layer 3, etching, forming the electrodes, and forming the reflection prevention film can be selected from conventional technologies. Also, the materials used are not restricted to those described above, and other materials that have been used conventionally in the past can be used. Also, apart from the silicon oxide film described above, the reflection-prevention film can also be a known reflection-prevention film such as a titanium oxide film.

[0036] Next will be described a structure of and method for making an inexpensive resin mold light-receiving semiconductor module 20 suited for mass production and that uses the light-receiving semiconductor device 10 made as a solar cell as described above. Referring to Fig. 13 through Fig. 16, the structure will be described first.

[0037] The light-receiving semiconductor module 20 can, for example, include: twenty-five light-receiving semiconductor devices 10; a conductive connector mechanism formed from six lead frames 29 and serving to electrically connect these twenty-five light-receiving semiconductor devices 10; a light transmitting member 31; a positive electrode terminal 33; and a negative electrode terminal 34.

[0038] The twenty-five spherical light-receiving semiconductor devices 10 are arranged in multiple rows and

10. A light-emitting or light-receiving semiconductor module as described in claim 7 wherein said first and second flat surfaces are formed with different diameters.
11. A light-emitting or light-receiving semiconductor module as described in claim 7 or claim 8 wherein said semiconductor element is formed from silicon semiconductor.
12. A light-emitting or light-receiving semiconductor module as described in claim 7 or claim 8 wherein said semiconductor element is formed from any one of compound semiconductor selected from GaAs, InP, GaP, GaN, or InCuSe.
13. A light-emitting or light-receiving semiconductor module as described in claim 7 or claim 8 wherein:
- said semiconductor element is formed from a p-type semiconductor;
- said diffusion layer is formed from a n-type diffusion layer; and
- said second flat surface is formed from a p-type recrystallized layer, said second electrode being disposed on a surface of said p-type recrystallized layer.
14. A light-emitting or light-receiving semiconductor module as described in claim 7 or claim 8 wherein:
- said semiconductor element is formed from a n-type semiconductor;
- said diffusion layer is formed from a p-type diffusion layer; and
- said second flat surface is formed from a n-type recrystallized layer, said second electrode being disposed on a surface of said n-type recrystallized layer.
15. A light-emitting or light-receiving semiconductor module comprising:
- a plurality of particle-shaped semiconductor devices having light-emitting or light-receiving properties, said plurality of semiconductor devices being disposed in a plurality of columns with uniform conductive orientation and being disposed in ring formations at equal intervals along a perimeter; and
- a conductive connection mechanism connecting each of said columns of said plurality of semiconductor devices to be electrically in series and connecting each of said rings of said plurality of semiconductor devices to be electrically in parallel.
16. A light-emitting or light-receiving semiconductor module as described in claim 15 wherein:
- a cylindrical light-transmitting member formed from a transparent synthetic resin is provided; and
- said plurality of columns of semiconductor devices arranged in ring formations is embedded in perimeter walls of said light-transmitting member.
17. A light-emitting or light-receiving semiconductor module as described in claim 16 wherein an irregular reflection surface that irregularly reflects light is formed on an inner perimeter surface of said light-transmitting member.
18. A method for making a light-emitting or light-receiving semiconductor module comprising:
- a first step for preparing a plurality of lead frames formed from thin metal sheets and a plurality of particle-shaped semiconductor devices having light-emitting or light-receiving properties;
- a second step for assembling said plurality of semiconductor devices between said plurality of lead frames so that conductive orientation is uniform, arranging said semiconductor devices as a matrix with plural rows and plural columns, and connecting each column of said semiconductor devices via said lead frame to be electrically in series and connecting each row of said semiconductor devices via said lead frame to be electrically in parallel; and
- a third step for embedding said matrix of said plurality of semiconductor devices in a light-transmitting member formed from a transparent synthetic resin.
19. A method for making a light-emitting or light-receiving semiconductor module as described in claim 18 wherein, in said third step, partially cylindrical lenses are formed on either side of each of said columns of said semiconductor devices.
20. A method for making a light-emitting or light-receiving semiconductor module comprising:
- a first step for preparing a plurality of ring-shaped lead frames formed from thin metal sheets and a plurality of particle-shaped semiconductor devices having light-emitting or light-receiving properties;
- a second step for assembling said plurality of semiconductor devices between said plurality of lead frames so that conductive orientation is uniform, arranging said semiconductor devices in plural columns and in ring formations at equal

FIG. 1

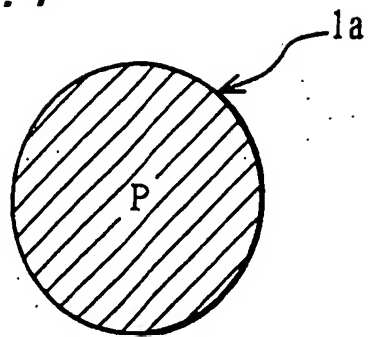


FIG. 2

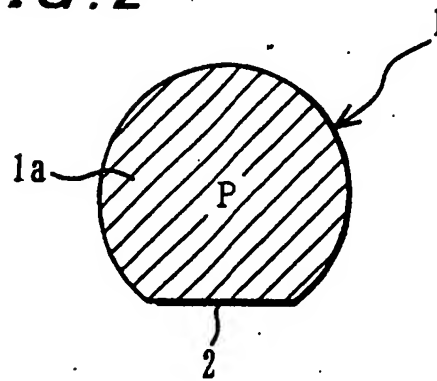
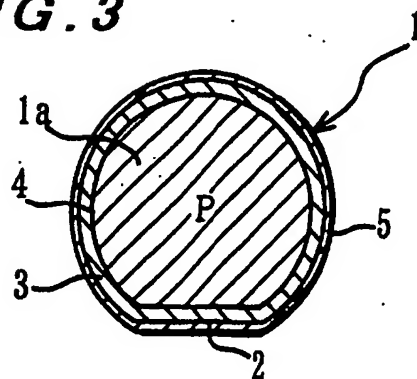


FIG. 3



intervals along a perimeter, and connecting
each column of said semiconductor devices via
said lead frame to be electrically in series and
connecting each ring of said semiconductor de-
vices via said lead frame to be electrically in 5
parallel; and
a third step for embedding said plurality of col-
umns of said plurality of semiconductor devices
in a cylindrical light-transmitting member
formed from a transparent synthetic resin. 10

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FIG. 7

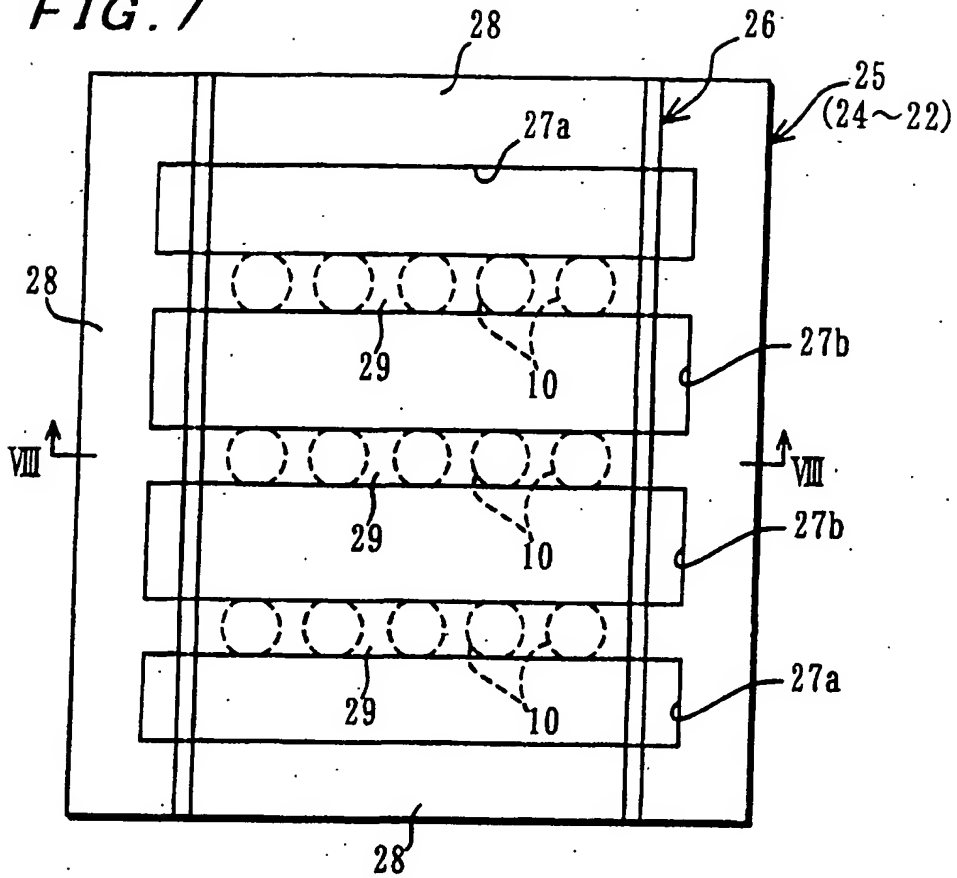


FIG. 8

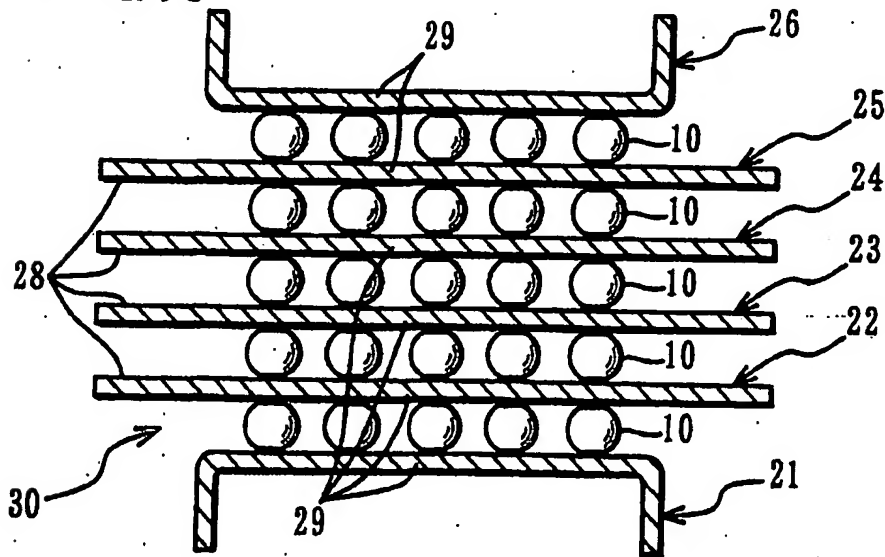


FIG. 4

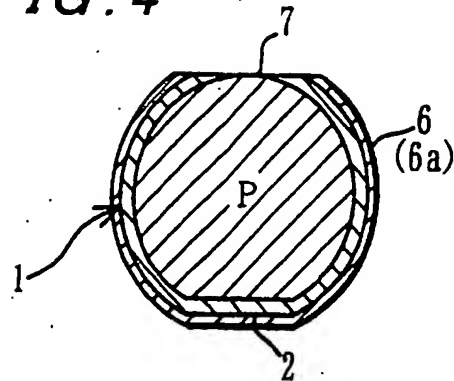


FIG. 5

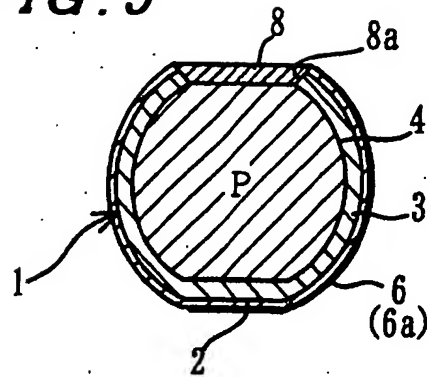


FIG. 6

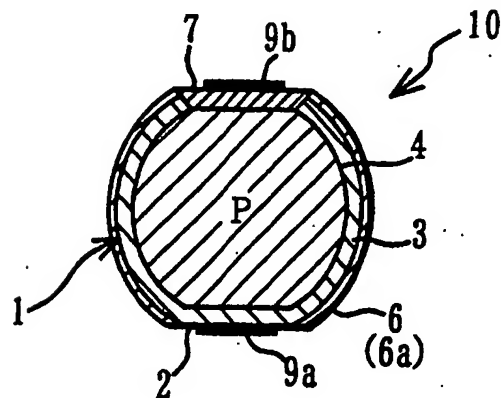


FIG. 13

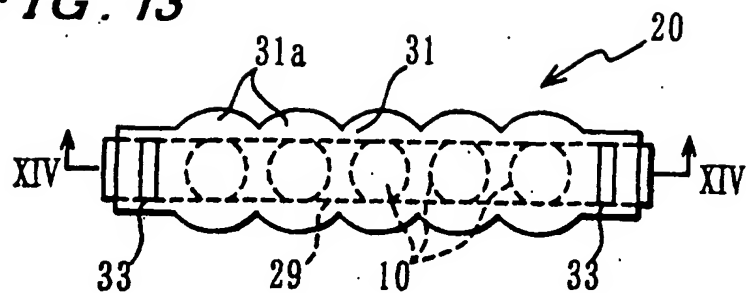


FIG. 14

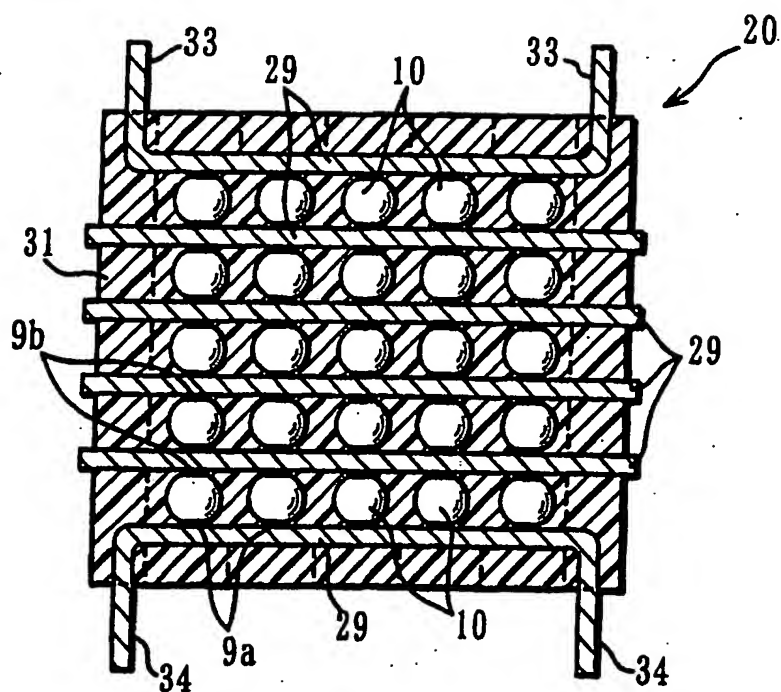


FIG. 15

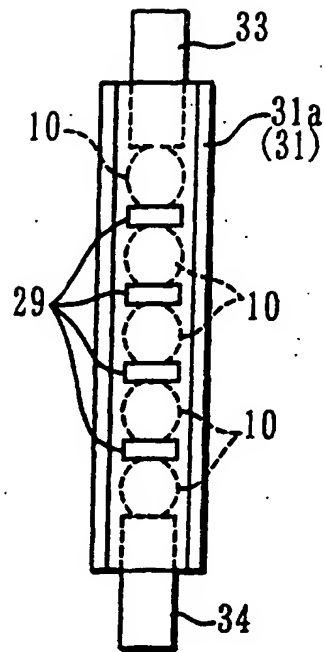


FIG. 16

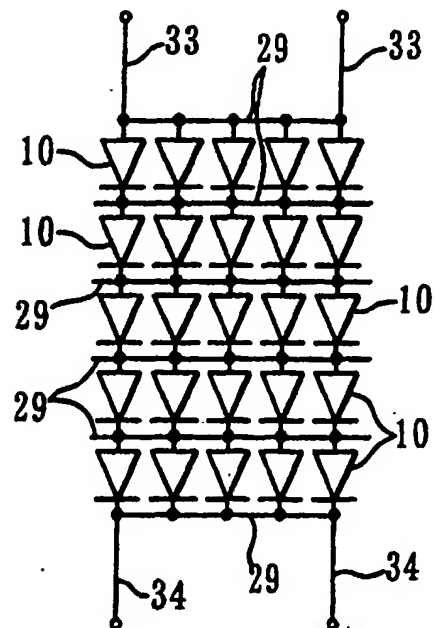


FIG. 17

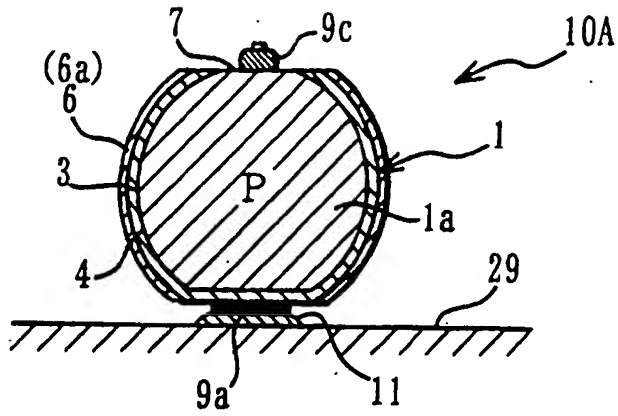


FIG. 18

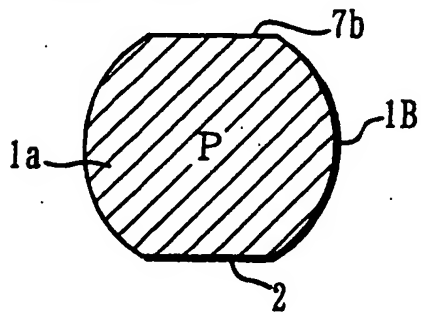


FIG. 20

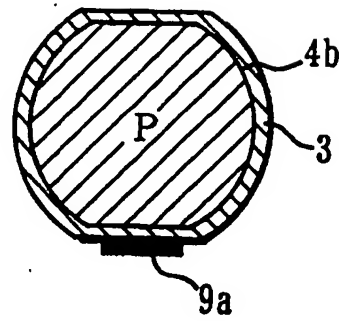


FIG. 19

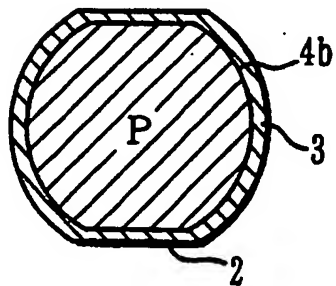


FIG. 21

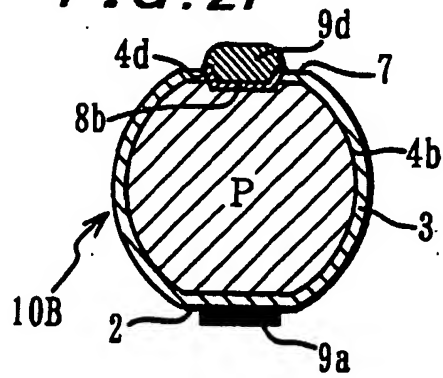


FIG. 22

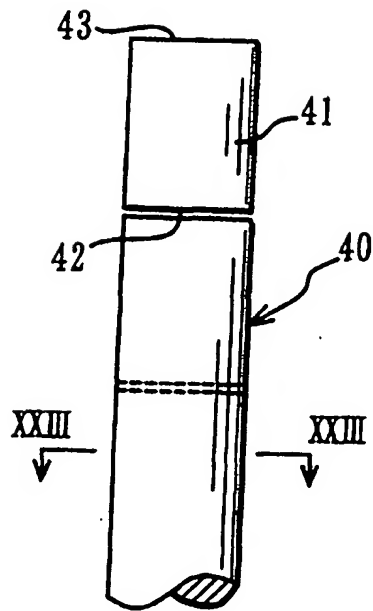


FIG. 23

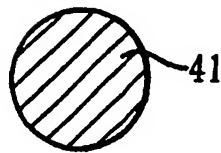


FIG. 28

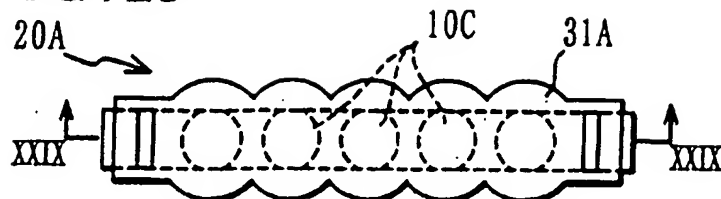


FIG. 29

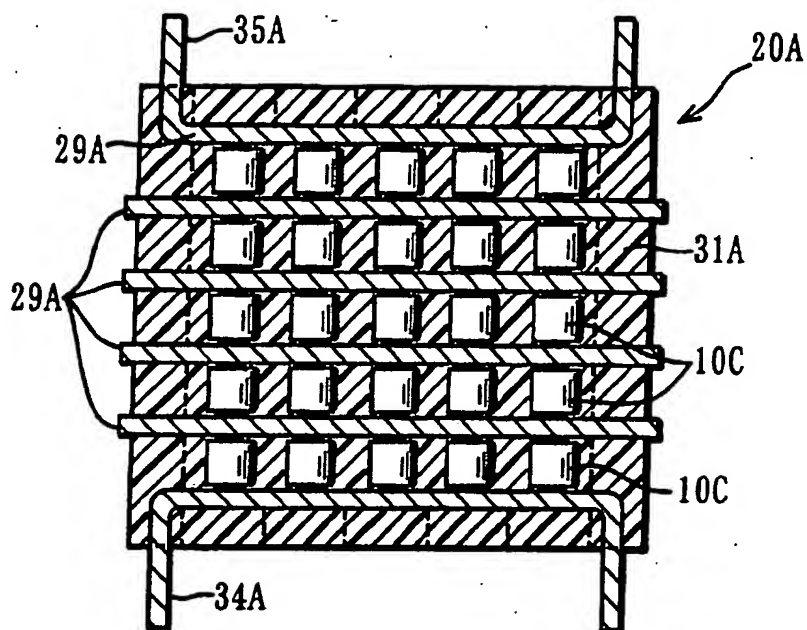


FIG. 30

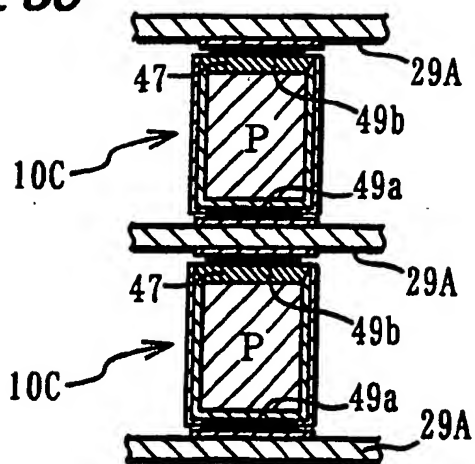


FIG. 24

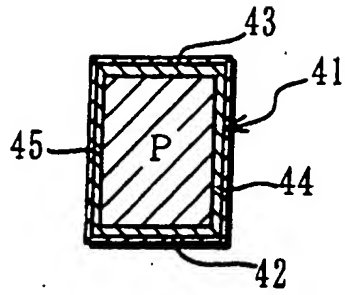


FIG. 25

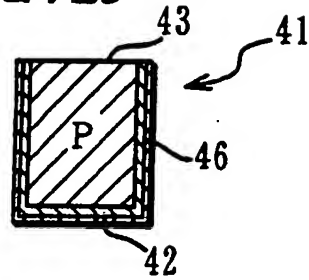


FIG. 26

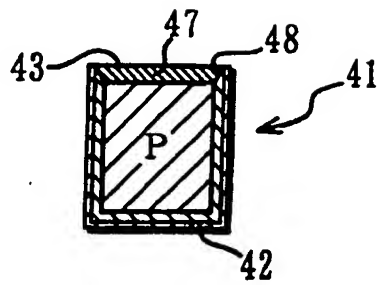


FIG. 27

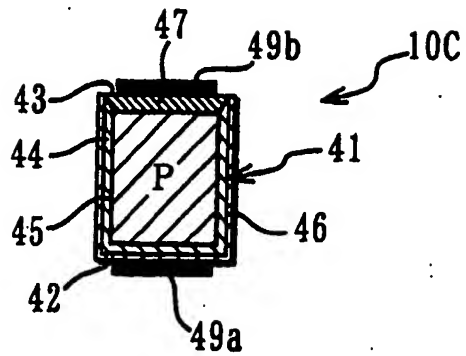


FIG. 33

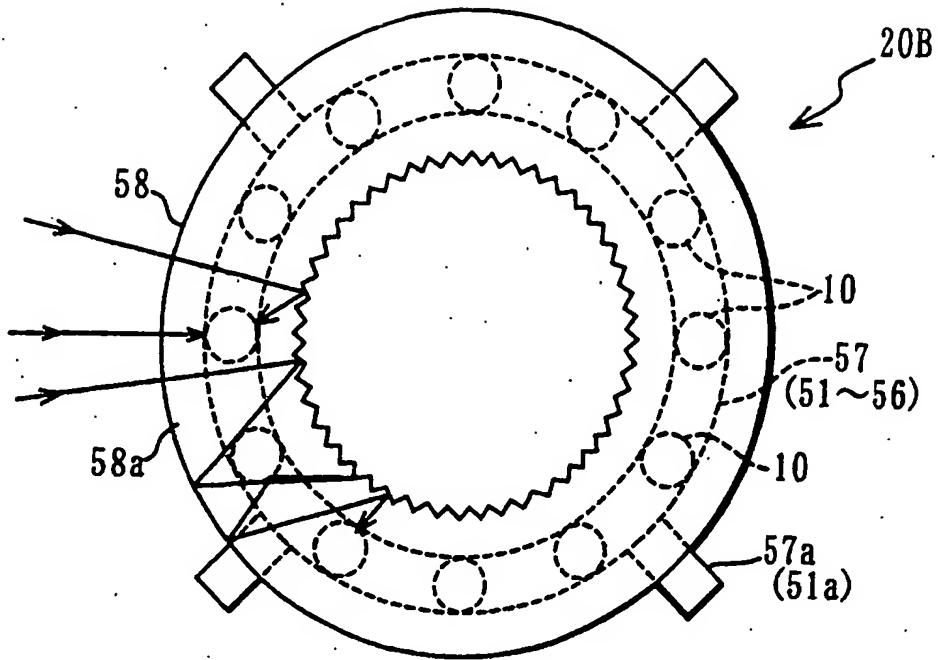
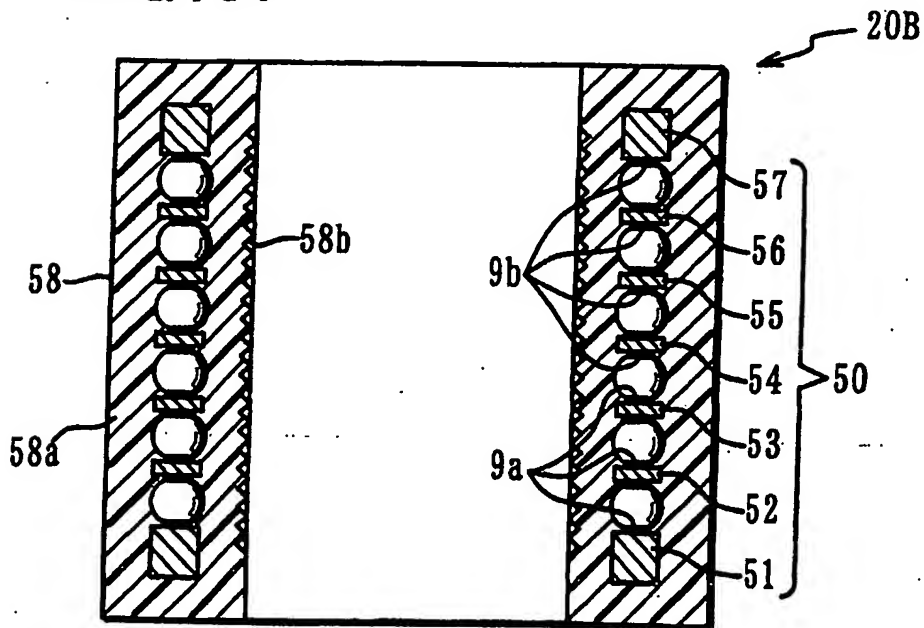


FIG. 34



INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP00/07360

A. CLASSIFICATION OF SUBJECT MATTER

Int. Cl.⁷ H01L31/042, H01L33/00, H01L25/04

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int. Cl.⁷ H01L31/04-31/078, H01L33/00, H01L25/00-25/13

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Jitsuyo Shinan Koho	1965-1996	Jitsuyo Shinan Toroku Koho	1996-2000
Kokai Jitsuyo Shinan Koho	1971-2000	Toroku Jitsuyo Shinan Koho	1994-2000

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 9-162434 A (Hitachi, Ltd.), 20 June, 1997 (20.06.97), Figs. 9, 10, 18 (Family: none)	1-20
Y	WO 98/15983 (Josuke NAKATA), 16 April, 1998 (16.04.98), Fig. 26 & AU, 7227896, A & CA, 2239626, A & EP, 866506, A1 & AU, 715515, B	1-20
Y	JP 3-85755 A (Toshiba Corporation), 10 April, 1991 (10.04.91), Figs. 1, 2 (Family: none)	1-20
Y	JP 4-293261 A (Fuji Electric Co., Ltd.), 16 October, 1992 (16.10.92), Figs. 1 to 5 (Family: none)	1-20

☒ Further documents are listed in the continuation of Box C.
 ☐ See patent family annex.

* Special categories of cited documents:	"I" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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"B" earlier document but published on or after the international filing date	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&" document member of the same patent family
"O" document referring to an oral disclosure, use, exhibition or other means	
"P" document published prior to the international filing date but later than the priority date claimed	

 Date of the actual completion of the international search
 26 January, 2001 (26.01.01)

 Date of mailing of the international search report
 06 February, 2001 (06.02.01)

 Name and mailing address of the ISA/
 Japanese Patent Office

Authorized officer

Facsimile No.

Telephone No.

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP00/07360

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 51-6686 A (Hitachi, Ltd.), 20 January, 1976 (20.01.76), Figs. 4 to 6 (Family: none)	6, 8, 11-14
Y	WO 99/10935 A (Josuke NAKATA), 04 March, 1999 (04.03.99), Figs. 1 to 10 & AU, 4031397, A & EP, 940860, A1	7-14
Y	JP 52-17229 A (Jack St. Claire Kilby), 09 February, 1977 (09.02.77), Figs. 11, 14 & SE, 7608483, A & NL, 7608131, A & DE, 2633878, A1 & FR, 2319962, A & US, 4021323, A & ES, 450191, A1 & AU, 1610776, A1 & US, 4100051, A & US, 4136436, A & AU, 498330, B2 & GB, 1561309, A & CA, 1073995, A1 & IT, 1066231, A	7-14
Y	JP 5-36997 A (Sanyo Electric Co., Ltd.), 12 February, 1993 (12.02.93), Fig. 2 (Family: none)	7-14
Y	US 4691076 A (Texas Instruments Incorporated), 01 September, 1987 (01.09.87), Fig. 1 & JP, 61-124179, A & CN, 86100381, A & IN, 164227, A & US, 4806495, A1 & CN, 1041244, A & CN, 1042275, A & CN, 1044874, A & JP, 6-13633, A	7-14

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